DMA055FHNMCMI-2A PRODUCT SPECIFICATION

Version 0.1 Feb 03, 2025

Customer's Approval						
<u>Signature</u>	<u>Date</u>					

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Approved by Eric Wan

Revision History

VERSION	DATE	DESCRIPTION	AUTHOR
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1. General Description

1.1 Introduction

This is a 5.44" size colour AMOLED display module. The display is 16.7M colour, has a resolution of 1080 x 1920 and supports MIPI interface and tape bonding on-cell touch panel.

1.2 Main Features

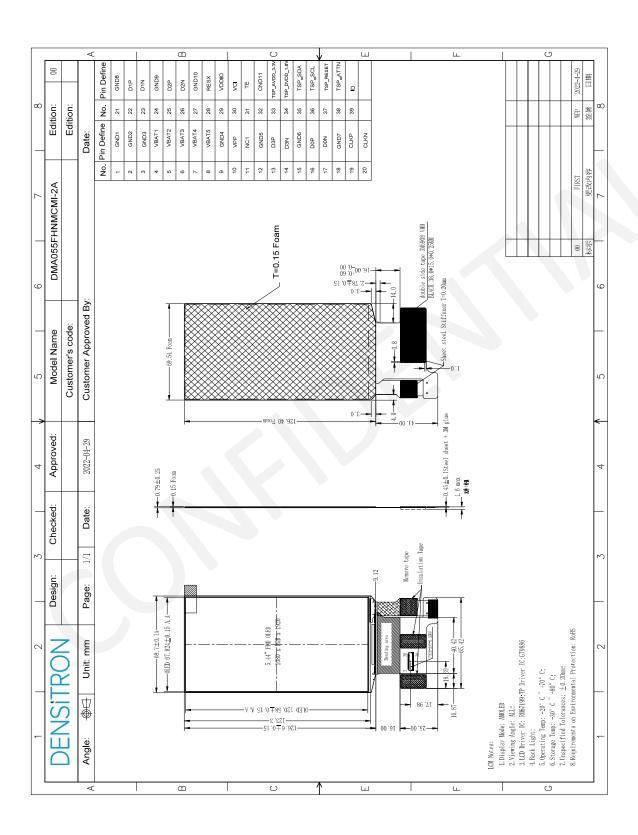
Item	Contents				
Display Type	AMOLED				
Screen Size	5.44" Diagonal				
Display Format	1080 x RGB x 1920 Dots				
No. of Colour	16.7M				
Mode	AMOLED				
Overall Dimensions	69.70 (W) x 126.60 (H) x 0.79 (D) mm				
Active Area	67.824 (W) x 120.58 (H) mm				
Surface Treatment	Glare (6H)				
Viewing Direction	All round				
Interface	MIPI				
Display Driver IC	RM67199				
Touch Panel	On cell				
Touch Interface	I ² C				
Touch Driver IC	GT9886				
Operating Temperature	-20°C ~ +70°C				
Storage Temperature	-30°C ~ +80°C				
ROHS	RoHS Compliance				

2. Mechanical Specification

2.1 Mechanical Characteristics

Item	Characteristic	Unit
Display Format	1080 x RGB x 1920	Dots
Overall Dimensions	69.70 (W) x 126.60 (H) x 0.79 (D)	mm
Active Area	67.824 (W) x 120.58 (H)	mm
Dot Pitch	0.0314 (W) x 0.0628 (H)	mm
Weight	TBD	g
IC Controller/Driver	RM67199	

2.2 Mechanical Drawing



3. Electrical Specification OLED

3.1 Absolute Maximum Rating

(Ta=25°C)

Item	Symbol	Min	Max	Unit
	VBAT	2.5	5.0	V
	VCC	-0.3	5.5	V
Power Voltage	VDDIO	-0.3	5.5	V
	TSP_AVDD_3.3V	-0.3	4.2	V
	TSP_DVDD_1.8V	-0.3	4.2	V
Operating Temperature	Тор	-20	+70	°C
Storage Temperature	T _{ST}	-30	+80	°C
Operating and Storage Humidity	H _{stg}	10%	90%	RH

Note 1: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3.2 "DC Electrical Characteristics OLED" and Section 4 "Optical Characteristics OLED." If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

3.2 DC Electrical Characteristics

(VCI=3.3V, GND=0V, Ta=25°C)

ltem	Symbol	Min	Тур	Max	Unit	Note
Power Voltage	VBAT	2.9	4.2	4.5	V	-
Digital Supply Voltage	VDDIO	1.65	1.8	3.3	V	-
Analog Supply Voltage	VCI	2.5	2.8	3.3	V	-
TD Dawer	TSP_AVDD_3.3V	2.7	3.0	3.4	V	-
TP Power	TSP_DVDD_1.8V	1.65	1.8	3.3	V	-
Loyal input Valtaga	Vih	0.7 IOVCC	-	IOVCC	V	-
Level input Voltage	V _{IL}	0	-	0.3 IOVCC	V	-
Current of Power Voltage	VBAT	-	205	380	mA	350 nits @gray 255
Current of digital supply voltage	Ivddio		-	10	mA	-
Current of analog supply voltage	lvcı	-	50	60	mA	VCI = 3.3V, @ Gray 255

3.3 Interface Pin Assignment

3.3.1 OLED Pin Assignment

1-3 GND1-3 P Ground 4-8 VBAT1-5 P Power supply (4.2V) 9 GND4 P Ground 10 VPP - Power supply for OTP. Float it for normal operation 11 NC1 - NC 12 GND5 P Ground 13 D3P I MIPI DSI differential data pair (Data lane 3) 14 D3N I MIPI DSI differential data pair (Data lane 3) 15 GND6 P Ground 16 D0P I/O MIPI DSI differential data pair (Data lane 0) 17 D0N I MIPI DSI differential data pair (Data lane 0) 18 GND7 P Ground 19 CLKP I MIPI DSI differential clock pair 20 CLKN I MIPI DSI differential clock pair 21 GND8 P Ground 22 D1P I MIPI DSI differential data pair (Data lane 1) 23 D1N I MIPI DSI differential data pair (Data lane 1) 24 GND9 P Ground 25 D2P I MIPI DSI differential data pair (Data lane 1) 26 D2N I MIPI DSI differential data pair (Data lane 2) 27 GND10 P Ground 28 RESX I Reset signal, active low 29 VDD10 P Digital circuit I/O power supply 30 VCI P Power supply for Analog circuit 31 TE O Tearing effect 32 GND11 P Ground 33 TSP_AVDD_3.3V P Touch IC data signal 36 TSP_SCL I Touch IIC clock signal 37 TSP_RESET I Touch reset signal	No.	Symbol	I/O	Function
4-8 VBAT1-5 P Power supply (4.2V) 9 GND4 P Ground 10 VPP - Power supply for OTP. Float it for normal operation 11 NC1 - NC 12 GND5 P Ground 13 D3P I MIPI DSI differential data pair (Data lane 3) 14 D3N I MIPI DSI differential data pair (Data lane 3) 15 GND6 P Ground 16 D0P I/O MIPI DSI differential data pair (Data lane 0) 17 D0N I MIPI DSI differential data pair (Data lane 0) 18 GND7 P Ground 19 CLKP I MIPI DSI differential clock pair 20 CLKN I MIPI DSI differential data pair (Data lane 1) 21 GND8 P Ground 22 D1P I MIPI DSI differential data pair (Data lane 1) 23 D1N I MIPI DSI differential data pair (Data lane 1) 24 GND9 P Ground 25 D2P I MIPI DSI differential data pair (Data lane 2) 26 D2N I MIPI DSI differential data pair (Data lane 2) 27 GND10 P Ground 28 RESX I Reset signal, active low 29 VDD10 P Digital circuit I/O power supply 30 VCI P Power supply for Analog circuit 31 TE O Tearing effect 32 GND11 P Ground 33 TSP_AVDD_3.3V P Touch IC digital circuit I/O power supply 35 TSP_SDA I/O Touch IIC data signal 36 TSP_SCL I Touch IIC clock signal				
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19 CLKP I MIPI DSI differential clock pair 20 CLKN I MIPI DSI differential clock pair 21 GND8 P Ground 22 D1P I MIPI DSI differential data pair (Data lane 1) 23 D1N I MIPI DSI differential data pair (Data lane 1) 24 GND9 P Ground 25 D2P I MIPI DSI differential data pair (Data lane 2) 26 D2N I MIPI DSI differential data pair (Data lane 2) 27 GND10 P Ground 28 RESX I Reset signal, active low 29 VDDIO P Digital circuit I/O power supply 30 VCI P Power supply for Analog circuit 31 TE O Tearing effect 32 GND11 P Ground 33 TSP_AVDD_3.3V P Touch IC analog power supply 35 TSP_SDA I/O Touch IIC data signal 36 TSP_SCL I Touch IIC clock signal	17	DON	I	MIPI DSI differential data pair (Data lane 0)
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21 GND8 P Ground 22 D1P I MIPI DSI differential data pair (Data lane 1) 23 D1N I MIPI DSI differential data pair (Data lane 1) 24 GND9 P Ground 25 D2P I MIPI DSI differential data pair (Data lane 2) 26 D2N I MIPI DSI differential data pair (Data lane 2) 27 GND10 P Ground 28 RESX I Reset signal, active low 29 VDDIO P Digital circuit I/O power supply 30 VCI P Power supply for Analog circuit 31 TE O Tearing effect 32 GND11 P Ground 33 TSP_AVDD_3.3V P Touch IC analog power supply (3.3V) 34 TSP_DVDD_1.8V P Touch IC data signal 36 TSP_SDA I/O Touch IIC data signal	19	CLKP	I	MIPI DSI differential clock pair
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24 GND9 P Ground 25 D2P I MIPI DSI differential data pair (Data lane 2) 26 D2N I MIPI DSI differential data pair (Data lane 2) 27 GND10 P Ground 28 RESX I Reset signal, active low 29 VDDIO P Digital circuit I/O power supply 30 VCI P Power supply for Analog circuit 31 TE O Tearing effect 32 GND11 P Ground 33 TSP_AVDD_3.3V P Touch IC analog power supply (3.3V) 34 TSP_DVDD_1.8V P Touch IC digital circuit I/O power supply 35 TSP_SDA I/O Touch IIC data signal 36 TSP_SCL I Touch IIC clock signal	22	D1P	I	MIPI DSI differential data pair (Data lane 1)
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26 D2N I MIPI DSI differential data pair (Data lane 2) 27 GND10 P Ground 28 RESX I Reset signal, active low 29 VDDIO P Digital circuit I/O power supply 30 VCI P Power supply for Analog circuit 31 TE O Tearing effect 32 GND11 P Ground 33 TSP_AVDD_3.3V P Touch IC analog power supply (3.3V) 34 TSP_DVDD_1.8V P Touch IC digital circuit I/O power supply 35 TSP_SDA I/O Touch IIC data signal 36 TSP_SCL I Touch IIC clock signal	24	GND9	Р	Ground
27 GND10 P Ground 28 RESX I Reset signal, active low 29 VDDIO P Digital circuit I/O power supply 30 VCI P Power supply for Analog circuit 31 TE O Tearing effect 32 GND11 P Ground 33 TSP_AVDD_3.3V P Touch IC analog power supply (3.3V) 34 TSP_DVDD_1.8V P Touch IC digital circuit I/O power supply 35 TSP_SDA I/O Touch IIC data signal 36 TSP_SCL I Touch IIC clock signal	25	D2P	I	MIPI DSI differential data pair (Data lane 2)
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30 VCI P Power supply for Analog circuit 31 TE O Tearing effect 32 GND11 P Ground 33 TSP_AVDD_3.3V P Touch IC analog power supply (3.3V) 34 TSP_DVDD_1.8V P Touch IC digital circuit I/O power supply 35 TSP_SDA I/O Touch IIC data signal 36 TSP_SCL I Touch IIC clock signal	28	RESX	ı	Reset signal, active low
31 TE O Tearing effect 32 GND11 P Ground 33 TSP_AVDD_3.3V P Touch IC analog power supply (3.3V) 34 TSP_DVDD_1.8V P Touch IC digital circuit I/O power supply 35 TSP_SDA I/O Touch IIC data signal 36 TSP_SCL I Touch IIC clock signal	29	VDDIO	Р	Digital circuit I/O power supply
32 GND11 P Ground 33 TSP_AVDD_3.3V P Touch IC analog power supply (3.3V) 34 TSP_DVDD_1.8V P Touch IC digital circuit I/O power supply 35 TSP_SDA I/O Touch IIC data signal 36 TSP_SCL I Touch IIC clock signal	30	VCI	Р	Power supply for Analog circuit
33 TSP_AVDD_3.3V P Touch IC analog power supply (3.3V) 34 TSP_DVDD_1.8V P Touch IC digital circuit I/O power supply 35 TSP_SDA I/O Touch IIC data signal 36 TSP_SCL I Touch IIC clock signal	31	TE	0	Tearing effect
34 TSP_DVDD_1.8V P Touch IC digital circuit I/O power supply 35 TSP_SDA I/O Touch IIC data signal 36 TSP_SCL I Touch IIC clock signal	32	GND11	Р	Ground
35 TSP_SDA I/O Touch IIC data signal 36 TSP_SCL I Touch IIC clock signal	33	TSP_AVDD_3.3V	Р	Touch IC analog power supply (3.3V)
36 TSP_SCL I Touch IIC clock signal	34	TSP_DVDD_1.8V	Р	Touch IC digital circuit I/O power supply
	35	TSP_SDA	I/O	Touch IIC data signal
37 TSP_RESET I Touch reset signal	36	TSP_SCL	ı	Touch IIC clock signal
	37	TSP_RESET	ı	Touch reset signal

No.	Symbol	I/O	Function
38	TSP_ATTN	I	Touch interrupt (1.8V)
39	ID	0	ID signal

I---Input, O---Output, P--- Power/Ground

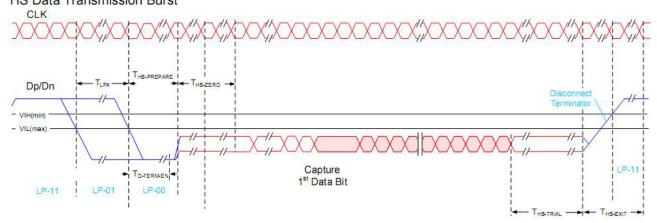
3.4 Block Diagram

TBD

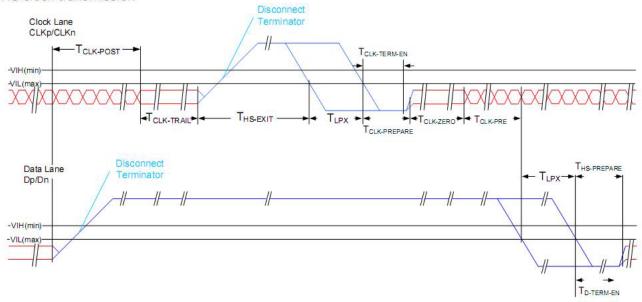
3.5 Timing Characteristics

3.5.1 DSI Interface Timing Characteristics

HS Data Transmission Burst

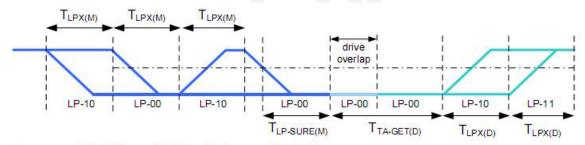


HS clock transmission

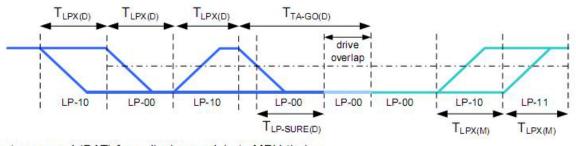


Parameter	Description	Min	Max	Unit
	Time that the transmitter continues to send HS clock after the last			
T _{CLK-POST}	associated Data Lane has transitioned to LP mode. Interval is defined	60ns + 52UI	-	ns
	as the period from the end of THS-TRAIL to the beginning of $T_{\text{CLK-TRAIL}}$.			
т	Time that the transmitter drives the HS-0 state after the last payload	60	-	
T _{CLK} -trail	clock bit of a HS transmission burst	60		ns
T _{HS-EXIT}	Time that the transmitter drives LP-11 following a HS burst	300	-	ns
_	Time for the Clock Lane receiver to enable the HS line termination,	Time for Dn	20	
T _{CLK} -term-en	starting from the time point when Dn crosses VIL.MAX.	to reach	38	ns

Parameter	Description	Min	Max	Unit
		V _{TERM-EN}		
TCLK-PREPARE	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	38	95	ns
T _{CLK-PRE}	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	UI
T _{CLK-PREPARE} + T _{CLK-ZERO}	TCLK-PREPART + time that the transmitter drives the HS-0 state prior to starting the Clock	300	-	ns
T _{D-TERM-EN}	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{\text{IL.MAX}}$.	Time for Dn to reach V _{TERM-EN}	35ns + 4UI	ns
Ths-prepare	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4UI	85ns + 6UI	ns
T _{HS-PREPARE} +	THS-PREPARE + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence	145ns + 10UI	-	ns
T _{HS} -trail	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	60ns + 4UI	-	ns



Bus turnaround (BAT) from MPU to display module timing



Bus turnaround (BAT) from display module to MPU timing

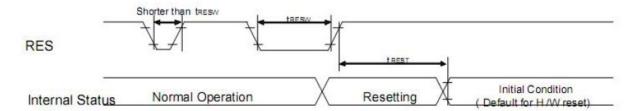
Low Power Mode

Parameter	Description	Min	Тур	Max	Unit	Note
T _{LPX(M)}	Transmitted length of any -Low-Power state period of MCU to display module	50	-	150	ns	1, 2
Tta-sure(m)	Time that the display module waits after LP-10 state before transmitting the Bridge state (LP-00) during a Line Turnaround	T _{LPX(M)}	-	2 T _{LPX(M)}	ns	2
T _{LPX(D)}	Transmitted length of any Low-Power state period of display module to MCU	50	-	150	ns	1, 2
T _{TA-GET(D)}	Time that the display module drives the Bridge state (LP-00) after accepting control during a Link Turnaround	-	5 T _{LPX(D)}		ns	2
Tta-go(d)	Time that the display module drives the Bridge state (LP-00) before releasing control during a Link Turnaround	-	4 T _{LPX(D)}		ns	2
T _{TA} -sure(d)	Time that the MPU waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround	T _{LPX(D)}	-	2 T _{LPX(D)}	ns	2

Note 1: T_{LPX} is an internal state machine timing reference Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

Note 2: Transmitter-specific parameter.

3.5.2 Reset Input Timing



(IOVCC=1.65 to 3.6V, VDD=2.5 to 3.6V, AGND=DGND=0V, Ta=-40 to 85°C)

Symbol	Parameter	Related Pins	Description		Max	Unit
tresw	Reset Low Pulse Width	RESX	ESX -		-	us
treset	Docat Complete Time	-	When reset applied during Sleep in mode	-	5	ms
	Reset Complete Time	-	When reset applied during Sleep Out mode	-	120	us

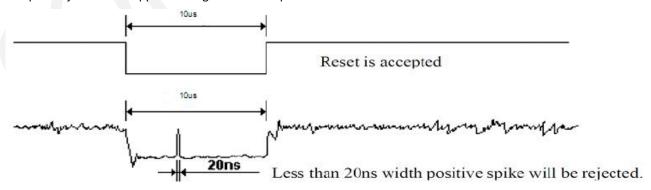
Note 1: Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action	
Shorter than 5us	Reset Rejected	
Longer than 10us	Reset	
Between 5us and 10us	Reset starts (It depends on voltage and temperature condition)	

Note 2: During the resetting period ,the display will be blanked (the display is entering blanking sequence, which maximum time is 120ms, when Reset Starts in Sleep Out-mode. The display remains the blank state in Sleep In-mode) and return to Default condition for H/W reset.

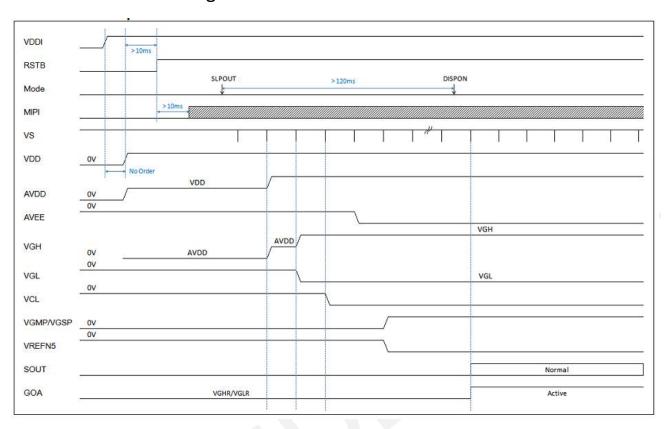
Note 3: During Reset Complete Time, data in OTP will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (tREST) within 5ms after a rising edge of RESX.

Note 4: Spike Rejection also applies during a valid reset pulse as shown below:

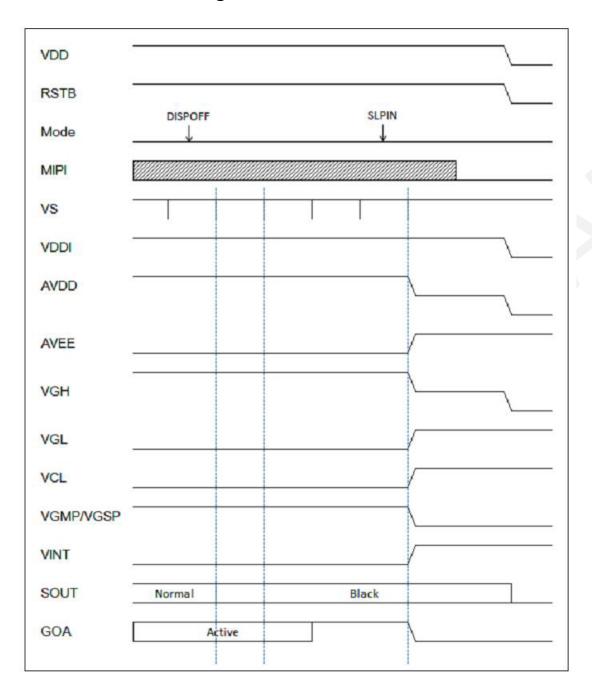


Note 5: It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

3.5.3 Power On Timing



3.5.4 Power Off Timing



4. Optical Specification OLED

4.1 Optical Characteristics

Charac	teristics	Symbol	Conditions	Min	Тур.	Max	Unit	Note
Contra	Contrast Ratio		θ = 0° Normal viewing angle	60000	-	-	-	1, 3
Respor	ise Time	Ton + Toff	25°C	-	-	2	ms	1, 4
<u>e</u>	Left	ΘL		80	-	-	Deg	2
g Ang	Right	ΘR	CD > 1000	80	-	-		
Viewing Angle	Тор	ΘU	CR ≥ 1000	80	-	-		
≒	Bottom	ΘD		80		-		
		Rx		0.660	0.690	0.720		
	Red	Ry		0.280	0.310	0.340	-	
icity		Gx		0.195	0.235	0.275		1, 5 1, 7 1, 6
omat	Green	Gy		0.680	0.720	0.760		
Colour Chromaticity		Вх	Backlight is on	0.113	0.143	0.173	-	1, 5
Color	Blue	Ву		0.014	0.044	0.074	-	
		Wx		0.275	0.295	0.315	-	
	White	Wy		0.285	0.305	0.325		
Lumi	Luminance		-	315	350	385	cd/m²	1, 7
Unifo	ormity	U	-	75	-	-	%	1, 6
N ⁻	NTSC		-	90	109	-	%	5

Measuring Condition = Ta is $25 \pm 3^{\circ}$ C, humidity is $65 \pm 20\%$ RH, dark room.

Note	ltem	Test method				
1	Definition of Optical Measurement System	Photo detector Field Contrast Ratio Luminance Chromaticity Lum Uniformity Response Time BM-7A 2° The center of the screen				
2	Definition of Viewing Angle Range and Measurement System	Viewing angle is measured at the center point of the OLED by CONOSCOPE(ergo-80) Normal line $\theta = \Phi = 0^{\circ}$ 12 o'clock direction $\Phi = 180^{\circ}$ Active Area $\Phi = 270^{\circ}$ 6 o'clock direction				
3	Definition of Contrast Ratio	Contrast Ratio (CR) = Luminance When AMOLED is at "White" state Luminance When AMOLED is at "Black" state "White state ": The state is that the OLED should drive by Vwhite. "Black state": The state is that the OLED should drive by Vblack. Vwhite: To be determined Vblack: To be determined.				
4	Definition of Response Time	The response time is defined as the OLED optical switching time interval between "White" state and "Black" state. Rise time (TON) is the time between photo detector output intensity changed from 90% to 10%. And fall time (TOFF) is the time between photo detector output intensity changed from 10% to 90%.				

Note	Item	Test method			
		"Bright" "Dark" "Bright" 10 % 0 % Tf			
5	Definition of Color Chromaticity (CIE1931)	Color coordinates measured at center point of OLED.			
6	Definition of Luminance Uniformity	Active area is divided into 9 measuring areas (Refer Fig. 2). Every measuring point is placed at the center of each measuring area. Luminance Uniformity (U) = Lmin/ Lmax LActive area length W Active area width Luminance Uniformity (U) = Lmin/ Lmax LActive area length W Active area width Luminance Uniformity (U) = Lmin/ Lmax Linin: The measured Maximum luminance of all measurement position.			

Note	ltem	Test method
7	Definition of Luminance	Measure the luminance of white state at center point.

5. Packaging

TBD

6. Quality Assurance Specification

6.1 Conformity

The performance, function and reliability of the shipped products conform to the Product Specification.

6.2 Dealing with Customer Complaints

6.2.1 Non-conforming Analysis

Purchaser should supply Densitron with detailed data of non-conforming sample.

After accepting it, Densitron should complete the analysis in reasonable time and update the status to the purchaser.

6.2.2 Handling of Non-conforming Displays

If any non-conforming displays are found during customer acceptance inspection which Densitron is clearly responsible for, return them to Densitron.

Both Densitron and customer should analyse the reason and discuss the handling of non-conforming displays when the reason is not clear.

Equally, both sides should discuss and come to agreement for issues pertaining to modification of Densitron quality assurance standard.

7. Reliability Specification

7.1 Reliability Tests

Test Item	Test Condition	Inspection after test		
High Temperature Operation	Ts = 70°C, 120 hrs			
Low Temperature Operation	Ta = -20°C, 120 hrs			
High Temperature Storage	Ta = 85°C, 120 hrs	No abnormalities in		
Low Temperature Storage	Ta = -40°C, 120 hrs	functions		
High Temperature & High Humidity Operating	Ta = +60°C, 93% RH ,120 hrs			
		Start with cold		
Thermal Shock	-40°C, 30 min. \leftrightarrow 85 $^{\circ}$ C , 30 min.	temperature.		
(Non-operation)	Change time: 5min. 32 cycles	End with high		
		temperature		
	C=150pF, R=330Ω,5point/panel			
	Air: ±4Kv, 20times.			
ESD	Contact: ±4Kv,20times	No abnormalities in functions		
	(Environment:15°C~35°C, 30%~60%,	TUTICLIOTIS		
	86Kpa~106Kpa)			

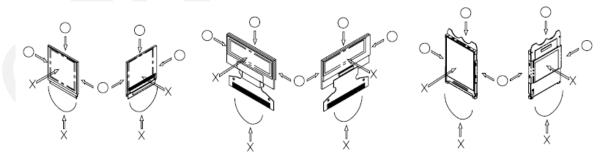
7.1.1 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23 ± 5 °C; $55\pm15\%$ RH.

8. Handling Precautions

8.1 Handling Precautions

- 1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
- 2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
- 3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
- 4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
- 5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
 - a. Scotch Mending Tape No. 810 or an equivalent
 - b. Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
 - c. Also, pay attention that the following liquid and solvent may spoil the polarizer:
 - Water
 - Ketone
 - Aromatic Solvents
- 6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



- 7) Do not apply stress to the LSI chips and the surrounding molded sections.
- 8) Do not disassemble nor modify the OEL display module.
- 9) Do not apply input signals while the logic power is off.
- 10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
 - Be sure to make human body grounding when handling OEL display modules.

- Be sure to ground tools to use or assembly such as soldering irons.
- To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
- Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
- 11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
- 12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

- 1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps, etc. and, also, avoiding high temperature and high humidity environments or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Densitron Technologies Plc.) At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
- 2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

- The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these
 values are exceeded, panel damage may be happen.
- 2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
- 3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
- 4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
- 5) As for EMI, take necessary measures on the equipment side basically.
- 6) When fastening the OEL display module, fasten the external plastic housing section.
- 7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
- 8) The electric potential to be connected to the rear face of the IC chip should be as follows: US2066

*Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4 Operation Precautions

- 1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur. Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
- 2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
 - a. Pins and electrodes
 - b. Pattern layouts such as the FPC
- 3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
 - a. Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
 - Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
- 4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
- 5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

8.5 Other Precautions

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.